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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	AUGUSTO MARQUES, ET AL.
Filed:	February 19, 2002
For:	APPARATUS AND METHODS FOR OUTPUT BUFFER CIRCUITRY WITH CONSTANT OUTPUT POWER IN RADIO-FREQUENCY CIRCUITRY
Serial No.:	10/079,058
Group Art Unit:	UNKNOWN
Examiner:	UNKNOWN
Atty Docket No.:	SILA:099

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on the date below:

5-20-02 Diane C Potts
Date Name

Assistant Commissioner For Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Please amend the application as follows.

In the specification:

The rewritten clean versions of all the specification changes are provided below. Attached at the end of this paper is an Appendix providing an indication of the changes relative to the prior version of the specification, as now required by Rule 121.

Please replace the paragraph beginning on page 2, line 1 and ending on page 3, line 2 with the following:

Furthermore, this patent application incorporates by reference the following patent documents: U.S. Patent Application Serial No. 09/708,339, Attorney Docket No.

SILA:035C1, titled "Method and Apparatus for Operating a PLL with a Phase Detector/Sample Hold Circuit for Synthesizing High-Frequency Signals for Wireless Communications," filed on November 8, 2000; U.S. Patent Application Serial No. 10/075,122, Attorney Docket No. SILA:078, titled "Digital Architecture for Radio-Frequency Apparatus and Associated Methods"; U.S. Patent Application Serial No. 10/075,099, Attorney Docket No. SILA:097, titled "Notch Filter for DC Offset Reduction in Radio-Frequency Apparatus and Associated Methods"; U.S. Patent Application Serial No. 10/074,676, Attorney Docket No. SILA:098, titled "DC Offset Reduction in Radio-Frequency Apparatus and Associated Methods"; U.S. Patent Application Serial No. 10/075,094, Attorney Docket No. SILA:074, titled "Radio-Frequency Communication Apparatus and Associated Methods"; U.S. Patent Application Serial No. 10/075,098, Attorney Docket No. SILA:075, titled "Apparatus and Methods for Generating Radio Frequencies in Communication Circuitry"; U.S. Patent Application Serial No. 10/074,591, Attorney Docket No. SILA:096, titled "Apparatus for Generating Multiple Radio Frequencies in Communication Circuitry and Associated Methods"; U.S. Patent Application Serial No. 10/079,057, Attorney Docket No. SILA:107, titled "Apparatus and Method for Front-End Circuitry in Radio-Frequency Apparatus"; and Provisional U.S. Patent Application Serial No. 60/333,664, Attorney Docket No. SILA:099PZ1, titled "Output Buffer Output Buffer for Local Oscillator and Synthesizer," filed on November 27, 2001.

In the Claims:

Please cancel claim 2.

Please add claims 3-42.

The rewritten clean versions of all the pending claims are provided below. Attached at the end of this paper is an Appendix providing an indication of the changes relative to the prior version of the claims, as now required by Rule 121(c).

1. A buffer circuitry for buffering a radio-frequency (RF) signal, comprising:

a complementary pair of switches having an input terminal and output terminal, the input terminal of the complementary pair of switches configured to respond to the radio-frequency signal, the output terminal of the complementary pair of switches coupled to an output of the buffer circuitry; and

a power source, including a capacitor coupled to a current source, the power source coupled to the complementary pair of switches, the power source configured to supply power to the complementary pair of switches such that the buffer circuitry supplies a substantially constant power level at its output.

3. The buffer circuitry according to claim 1, wherein the input terminal of the complementary pair of switches receives the radio-frequency signal from a phase-lock loop circuitry coupled to the complementary pair of switches.

4. The buffer circuitry according to claim 3, wherein the current source supplies an output current that is substantially constant over semiconductor fabrication process and temperature variations.

5. The buffer circuitry according to claim 4, wherein the complementary pair of switches are capable of being controlled so as to power down the output of the buffer circuitry.

6. The buffer circuitry according to claim 5, wherein the current source comprises a programmable current source.

7. The buffer circuitry according to claim 6, wherein the power level at the output of the buffer circuitry may be configured by programming the output current of the current source.

8. The buffer circuitry according to claim 7, wherein the output current of the current source is programmable in response to a plurality of digital signals.

9. The buffer circuitry according to claim 8, wherein the complementary pair of switches comprises a series combination of a first switch and a second switch.

10. The buffer circuitry according to claim 9, wherein a first terminal of the series combination of the first and second switches receives the output current of the current source, and wherein a second terminal of the series combination of the first and second switches couples to a reference potential.

11. The buffer circuitry according to claim 10, wherein a first terminal of the capacitor couples to the first terminal of the combination of first and second switches, and wherein a second terminal of the capacitor couples to the reference potential.

12. The buffer circuitry according to claim 11, wherein the first and second switches comprise complementary metal oxide semiconductor circuitry.

13. The buffer circuitry according to claim 12, wherein the reference potential comprises a ground potential.

14. A radio-frequency (RF) apparatus, comprising:

a first integrated circuit, including a first buffer, the first buffer comprising:

a first switch network configured to accept a first input signal, the first switch network configured to supply a first output signal at a first output; and

a power source coupled to the first switch network, the power source configured to supply power to the first switch network such that the first switch network provides a substantially constant power at the first output.

15. The radio-frequency apparatus according to claim 14, wherein the first switch network comprises a pair of controllable switches configured to respond to the first input signal.

16. The radio-frequency apparatus according to claim 15, wherein the power source comprises a current source coupled to a capacitor.

17. The radio-frequency apparatus according to claim 16, wherein the first integrated circuit comprises local-oscillator circuitry.

18. The radio-frequency apparatus according to claim 17, wherein the current source provides a substantially constant current over temperature and semiconductor fabrication process variations.

19. The radio-frequency apparatus according to claim 18, wherein the current source comprises a programmable current source.

20. The radio-frequency apparatus according to claim 19, wherein the power level at the output of the buffer circuitry may be configured by programming the output current of the current source.

21. The radio-frequency apparatus according to claim 20, wherein the output current of the current source is programmable in response to a plurality of digital signals.

22. The radio-frequency apparatus according to claim 21, wherein the pair of controllable switches comprises complementary switches.

23. The radio-frequency apparatus according to claim 22, wherein the local-oscillator circuitry further comprises a phase-lock loop circuit, the phase-lock loop circuit configured to supply the first input signal to the first switch network.

24. The radio-frequency apparatus according to claim 23, further comprising radio-frequency receiver circuitry included within a second integrated circuit coupled to the

first integrated circuit, the radio-frequency receiver circuitry configured to receive a radio-frequency signal.

25. The radio-frequency apparatus according to claim 24, further comprising a third integrated circuit coupled to the second integrated circuit, the third integrated circuit including digital signal-processing circuitry configured to accept a digital output of the radio-frequency receiver circuitry.

26. The radio-frequency apparatus according to claim 14, wherein the first integrated circuit further comprises a second buffer, the second buffer including a second switch network coupled to the power source, the second switch network configured to accept a second input signal, the second switch network further configured to supply a second output signal at a second output, wherein the second switch network provides a substantially constant power at the second output.

27. The radio-frequency apparatus according to claim 26, wherein the first and second output signals comprise a differential output signal in response to a differential input signal supplied as the first and second input signals.

28. The radio-frequency apparatus according to claim 27, wherein the first and second buffers are further configured to be powered down selectively in response to a power-down signal.

29. The radio-frequency apparatus according to claim 28, wherein the power source comprises a current source, the current source configured to supply a substantially constant output current.

30. The radio-frequency apparatus according to claim 29, wherein the current source provides the substantially constant current over temperature and semiconductor fabrication process variations.

31. The radio-frequency apparatus according to claim 30, wherein the current source comprises a programmable current source.

32. The radio-frequency apparatus according to claim 31, wherein the power level at the output of the first and second switch networks may be configured by programming the output current of the current source.

33. The radio-frequency apparatus according to claim 32, wherein the output current of the current source is programmable in response to a plurality of digital signals.

34. A method of buffering a input radio-frequency (RF) input signal to generate a buffered radio-frequency signal, comprising:

accepting the radio-frequency signal as an input signal in a switch network;

generating the buffered radio-frequency signal at an output of the switch network; and

supplying power to the switch network by a power source so that the switch network has a substantially constant output power.

35. The method according to claim 34, wherein generating the buffered radio-frequency signal at an output of the switch network comprises using a pair of controllable switches configured to respond to the radio-frequency input signal.

36. The method according to claim 35, wherein supplying power to the switch network comprises including in the power source a current source coupled to a capacitor.

37. The method according to claim 36, further comprising receiving the radio-frequency input signal from a local-oscillator circuitry.

38. The method according to claim 37, wherein supplying power to the switch network comprises using the current source to provide a substantially constant current over temperature and semiconductor fabrication process variations.

39. The method according to claim 38, wherein supplying power to the switch network comprises programming the current provided by the current source.

40. The method according to claim 39, further comprising configuring the output power of the switch network by programming the current provided by the current source.

41. The method according to claim 40, further comprising using a plurality of digital signals to program the current provided by the current source.

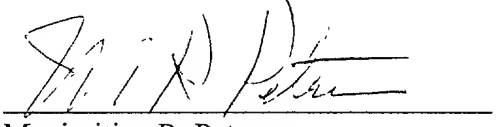
42. The method according to claim 41, wherein receiving the radio-frequency input signal from a local-oscillator circuitry further comprises receiving the input signal from a phase-lock loop circuit.

CONCLUSION

A check in the amount of $378.00 is enclosed for excess claims. Should any additional fees under 37 CFR 1.16-1.21 be required for any reason relating to the enclosed materials, the Commissioner is authorized to deduct such fees from Deposit Account No. 10-1205/SILA:099.

The examiner is invited to contact the undersigned at the phone number indicated below with any questions or comments, or to otherwise facilitate expeditious and compact prosecution of the application.

Respectfully submitted,



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APPENDIX

MARKED UP VERSION OF AMENDMENTS AS REQUIRED BY RULE 121

In The Specification:

Please replace the paragraph beginning on page 2, line 1 and ending on page 3, line 2 with the following:

--Furthermore, this patent application incorporates by reference the following patent documents: U.S. Patent Application Serial No. 09/708,339, Attorney Docket No. SILA:035C1, titled "Method and Apparatus for Operating a PLL with a Phase Detector/Sample Hold Circuit for Synthesizing High-Frequency Signals for Wireless Communications," filed on November 8, 2000; U.S. Patent Application Serial No. [____________] 10/075,122, Attorney Docket No. SILA:078, titled "Digital Architecture for Radio-Frequency Apparatus and Associated Methods"; U.S. Patent Application Serial No. [____________] 10/075,099, Attorney Docket No. SILA:097, titled "Notch Filter for DC Offset Reduction in Radio-Frequency Apparatus and Associated Methods"; U.S. Patent Application Serial No. [____________] 10/074,676, Attorney Docket No. SILA:098, titled "DC Offset Reduction in Radio-Frequency Apparatus and Associated Methods"; U.S. Patent Application Serial No. [____________] 10/075,094, Attorney Docket No. SILA:074, titled "Radio-Frequency Communication Apparatus and Associated Methods"; U.S. Patent Application Serial No.

[_____] 10/075,098, Attorney Docket No. SILA:075, titled "Apparatus and Methods for Generating Radio Frequencies in Communication Circuitry"; U.S. Patent Application Serial No. [_____] 10/074,591, Attorney Docket No. SILA:096, titled "Apparatus for Generating Multiple Radio Frequencies in Communication Circuitry and Associated Methods"; U.S. Patent Application Serial No. [_____] 10/079,057, Attorney Docket No. SILA:107, titled "Apparatus and Method for Front-End Circuitry in Radio-Frequency Apparatus"; and Provisional U.S. Patent Application Serial No. 60/333,664, Attorney Docket No. SILA:099PZ1, titled "Output Buffer Output Buffer for Local Oscillator and Synthesizer," filed on November 27, 2001.--

In The Claims:

Please cancel claim 2.

[2.(Canceled) A radio-frequency (RF) apparatus, comprising:

a first circuit partition, comprising receiver analog circuitry configured to produce a digital receive signal from an analog radio-frequency signal; and

a second circuit partition, comprising receiver digital circuitry configured to accept the digital receive signal, wherein the first and second circuit partitions are partitioned so that interference effects between the first circuit partition and the second circuit partition tend to be reduced.]

Please add new claims 3-42.

--3. (New) The buffer circuitry according to claim 1, wherein the input terminal of the complementary pair of switches receives the radio-frequency signal from a phase-lock loop circuitry coupled to the complementary pair of switches.

4. (New) The buffer circuitry according to claim 3, wherein the current source supplies an output current that is substantially constant over semiconductor fabrication process and temperature variations.

5. (New) The buffer circuitry according to claim 4, wherein the complementary pair of switches are capable of being controlled so as to power down the output of the buffer circuitry.

6. (New) The buffer circuitry according to claim 5, wherein the current source comprises a programmable current source.

7. (New) The buffer circuitry according to claim 6, wherein the power level at the output of the buffer circuitry may be configured by programming the output current of the current source.

8. (New) The buffer circuitry according to claim 7, wherein the output current of the current source is programmable in response to a plurality of digital signals.

9. (New) The buffer circuitry according to claim 8, wherein the complementary pair of switches comprises a series combination of a first switch and a second switch.

10. (New) The buffer circuitry according to claim 9, wherein a first terminal of the series combination of the first and second switches receives the output current of the current source, and wherein a second terminal of the series combination of the first and second switches couples to a reference potential.

11. (New) The buffer circuitry according to claim 10, wherein a first terminal of the capacitor couples to the first terminal of the combination of first and second switches, and wherein a second terminal of the capacitor couples to the reference potential.

12. (New) The buffer circuitry according to claim 11, wherein the first and second switches comprise complementary metal oxide semiconductor circuitry.

13. (New) The buffer circuitry according to claim 12, wherein the reference potential comprises a ground potential.

14. (New) A radio-frequency (RF) apparatus, comprising:

a first integrated circuit, including a first buffer, the first buffer comprising:

a first switch network configured to accept a first input signal, the first switch network configured to supply a first output signal at a first output; and

a power source coupled to the first switch network, the power source configured to supply power to the first switch network such that the first switch network provides a substantially constant power at the first output.

15. (New) The radio-frequency apparatus according to claim 14, wherein the first switch network comprises a pair of controllable switches configured to respond to the first input signal.

16. (New) The radio-frequency apparatus according to claim 15, wherein the power source comprises a current source coupled to a capacitor.

17. (New) The radio-frequency apparatus according to claim 16, wherein the first integrated circuit comprises local-oscillator circuitry.

18. (New) The radio-frequency apparatus according to claim 17, wherein the current source provides a substantially constant current over temperature and semiconductor fabrication process variations.

19. (New) The radio-frequency apparatus according to claim 18, wherein the current source comprises a programmable current source.

20. (New) The radio-frequency apparatus according to claim 19, wherein the power level at the output of the buffer circuitry may be configured by programming the output current of the current source.

21. (New) The radio-frequency apparatus according to claim 20, wherein the output current of the current source is programmable in response to a plurality of digital signals.

22. (New) The radio-frequency apparatus according to claim 21, wherein the pair of controllable switches comprises complementary switches.

23. (New) The radio-frequency apparatus according to claim 22, wherein the local-oscillator circuitry further comprises a phase-lock loop circuit, the phase-lock loop circuit configured to supply the first input signal to the first switch network.

24. (New) The radio-frequency apparatus according to claim 23, further comprising radio-frequency receiver circuitry included within a second integrated circuit coupled to the first integrated circuit, the radio-frequency receiver circuitry configured to receive a radio-frequency signal.

25. (New) The radio-frequency apparatus according to claim 24, further comprising a third integrated circuit coupled to the second integrated circuit, the third integrated circuit including digital signal-processing circuitry configured to accept a digital output of the radio-frequency receiver circuitry.

26. (New) The radio-frequency apparatus according to claim 14, wherein the first integrated circuit further comprises a second buffer, the second buffer including a second switch network coupled to the power source, the second switch network configured to accept a second input signal, the second switch network further configured to supply a second output signal at a second output, wherein the second switch network provides a substantially constant power at the second output.

27. (New) The radio-frequency apparatus according to claim 26, wherein the first and second output signals comprise a differential output signal in response to a differential input signal supplied as the first and second input signals.

28. (New) The radio-frequency apparatus according to claim 27, wherein the first and second buffers are further configured to be powered down selectively in response to a power-down signal.

29. (New) The radio-frequency apparatus according to claim 28, wherein the power source comprises a current source, the current source configured to supply a substantially constant output current.

30. (New) The radio-frequency apparatus according to claim 29, wherein the current source provides the substantially constant current over temperature and semiconductor fabrication process variations.

31. (New) The radio-frequency apparatus according to claim 30, wherein the current source comprises a programmable current source.

32. (New) The radio-frequency apparatus according to claim 31, wherein the power level at the output of the first and second switch networks may be configured by programming the output current of the current source.

33. (New) The radio-frequency apparatus according to claim 32, wherein the output current of the current source is programmable in response to a plurality of digital signals.

34. (New) A method of buffering a input radio-frequency (RF) input signal to generate a buffered radio-frequency signal, comprising:

accepting the radio-frequency signal as an input signal in a switch network;

generating the buffered radio-frequency signal at an output of the switch network; and

supplying power to the switch network by a power source so that the switch network has a substantially constant output power.

35. (New) The method according to claim 34, wherein generating the buffered radio-frequency signal at an output of the switch network comprises using a pair of controllable switches configured to respond to the radio-frequency input signal.

36. (New) The method according to claim 35, wherein supplying power to the switch network comprises including in the power source a current source coupled to a capacitor.

37. (New) The method according to claim 36, further comprising receiving the radio-frequency input signal from a local-oscillator circuitry.

38. (New) The method according to claim 37, wherein supplying power to the switch network comprises using the current source to provide a substantially constant current over temperature and semiconductor fabrication process variations.

39. (New) The method according to claim 38, wherein supplying power to the switch network comprises programming the current provided by the current source.

40. (New) The method according to claim 39, further comprising configuring the output power of the switch network by programming the current provided by the current source.

41. (New) The method according to claim 40, further comprising using a plurality of digital signals to program the current provided by the current source.

42. (New) The method according to claim 41, wherein receiving the radio-frequency input signal from a local-oscillator circuitry further comprises receiving the input signal from a phase-lock loop circuit.--